REMARKS

Claims 1-15 have been amended. No claims have been canceled or added. Accordingly, claims 1-15 are currently pending in the above-identified application.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority. Submitted herewith is a certified copy of the corresponding Japanese patent application 2000-175536, filed June 7, 2000). An indication that this document has been safely received would be appreciated.

Specification

The specification has been amended to cure minor grammatical and idiomatic informalities. No new matter has been added. The abstract has been rewritten into better form.

35 U.S.C. §112

The claims have been amended to overcome the Examiner's rejection under this section. The Examiner is hereby invited to contact the undersigned by telephone with any questions.

35 U.S.C. §§102 and 103

Claims 1-8 and 10-15 stand rejected under 35 U.S.C. §102(b) as being anticipated by Mitsushira et al (U.S. 5,325,489). Further, claim 9 is rejected under 35 U.S.C. §103(a) as being unpatentable over Mitsushira et al (U.S. 5,325,489). These rejections are traversed as follows.

The present invention is directed to a data transfer controller and a data processor including an arithmetic and logic controller and a data transfer controller. The data transfer controller reduces the processing load of a central processing unit (CPU), or the like, in updating data transfer control conditions during a series of sequential processes of receiving and storing data in a memory, or the like. The data transfer controller is capable of notifying the CPU each time a predetermined amount of data is stored in order to process already stored data in parallel with a subsequent data storing process.

According to the presently claimed invention, the data transfer controller continues data transfer without CPU control because the data transfer controller outputs an interrupt each time the data transfer reaches a predetermined amount and is capable of resetting the data transfer control conditions accordingly (see Fig. 1 and specification page 16,

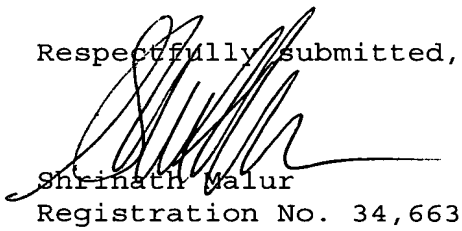
line 12 to page 20, line 16). As such, data processing efficiency is improved (See page 37, line 15 to page 38, line 15).

On the other hand, Mitsuhira et al disclose a data transfer control device in which a next area authorization bit 203 is set or reset for a subsequent DMA transfer area in the DMA transfer termination interrupt processing routine. This way, DMA transfer for the next area may be continuously executed or stopped when the DMA transfer presently being conducted is completed (see column 8, lines 48-62). However, Mitsuhira et al are silent regarding the resetting of data transfer control conditions in order to continuously transfer data after reaching an end address of a data transfer destination. As such, Mitsuhira et al are also silent regarding reducing the load on the CPU by reducing the amount of times the CPU has to repetitively set the data transfer conditions for a series of processes of sequentially storing received data in a memory, or the like. As such, it is submitted that the pending claims patentably define the present invention over the cited art.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



Shrinath Malur
Registration No. 34,663
Attorney for Applicant(s)

MATTINGLY, STANGER & MALUR
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
Date: April 29, 2004